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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/886,166	06/20/2001	Donald J. O' Riordan	CAD 334	5959

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EXAMINER	
PHAN, THAI Q	
ART UNIT	PAPER NUMBER
2128	

DATE MAILED: 06/13/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/886,166	O' RIORDAN ET AL.	
	Examiner	Art Unit	
	Thai Q. Phan	2128	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *18 February 2005*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-26* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *7-12 and 20-26* is/are allowed.

6)☐ Claim(s) *1-6 and 13-19* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *20 June 2001* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

This Office Action is in response to applicants' amendment filed on 02/18/2005. Claims 1-26 are pending in the action.

Claim Rejections - 35 USC § 103

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

2. Claims 1 and 13 are rejected under 35 U.S.C. 103(a) as being unpatentable over Sharrit (US patent no. 5,588,142) or Vlach, (US patent no. 4,985,860) or Kazmierski et al (US patent no. 6,110,217), in view of On et al, US patent no. 6,275,956 B1.

As per claim 1, Sharrit, Vlach, and Kazmierski disclose methods and simulators for simulating a circuit with feature limitations very similar to the claimed invention. According to Sharrit ,Vlach and Kazmierski, the method includes steps:

Performing a regular iterative equation solution process (Sharrit, col. 3, lines 7-42, col. 5, lines 31-43, for example) or (Vlach, col. 4, lines 43-65, col. 6, line 47 to col. 7, line 14, for example) or Kazmierski (cols. 6-10),

Performing process iteration at an accepted timepoint (Sharrit, col. 6, lines 21-43, col. 8, lines 43-59, for example), and user interacting with the process simulation during the iteration taking place (col. 5, line 30 to col. 6, line 44, col. 7, lines 3-55, col. 10, lines 33-50) or Vlach, col. 7, lines 1-22, col. 9, lines 9-27, for example, or Kazmierski (cols. 6-19). Sharrit, Vlach and Kazmierski do not expressly disclose the claimed limitation of a

replay of the last iteration. Such claimed replay of the iteration is well-known in the art. In fact, On teaches means and step to perform a replay of an iteration for independent process debugging and dynamically view or examine the debugging process (col. 4, lines 21-61, col. 5, lines 1-40).

This would motivate practitioner in the art at the time of the invention was made to combined the teaching of iteration process replay in On into Sharrit, Vlach or Kazmierski simulation in order to independently debug process error and dynamically examine process debugging. This advantage would improve the simulation process by replaying iteration process at the selected or accepted time point as taught in On.

As per claim 13, Sharrit, Vlach and Kazmierski disclose a computer readable medium for performing method steps and simulation function for simulating a circuit with feature limitations very similar to the claimed invention. According to Sharrit, Vlach and Kazmierski, the computer readable medium include means and functional steps:

Performing a regular iterative equation solution process (Sharrit, col. 3, lines 7-42, col. 5, lines 31-43, for example) or (Vlach, col. 4, lines 43-65, col. 6, line 47 to col. 7, line 14, for example) or Kazmierski (cols. 6-10),

Performing process iteration at an accepted timepoint (Sharrit, col. 6, lines 21-43, col. 8, lines 43-59, for example), and user interacting with the process simulation during the iteration taking place (col. 5, line 30 to col. 6, line 44, col. 7, lines 3-55, col. 10, lines 33-50) or Vlach, col. 7, lines 1-22, col. 9, lines 9-27, for example, or Kazmierski (cols. 6-19). Sharrit, Vlach and Kazmierski do not expressly disclose the claimed limitation of a replay of the last iteration. Such claimed replay of the iteration is well-known in the art.

In fact, On teaches means and step to perform a replay of iteration for independent process debugging and dynamically view or examine the debugging process (col. 4, lines 21-61, col. 5, lines 1-40).

This would motivate practitioner in the art at the time of the invention was made to combined the teaching of iteration process replay in On into Sharrit, Vlach or Kazmierski simulation in order to independently debug process error and dynamically examine process debugging.

3. Claims 2-6, and 14-19 are rejected under 35 U.S.C. 103(a) as being unpatentable over Sharrit, US patent no. 5,588,142, or Kazmierski (US patent no. 6,110,217) in view of On et al, US patent no. 6,275,956 B1.

As per claim 2, Sharrit and Kazmierski disclose methods and simulators for simulating a circuit with feature limitations very similar to the claimed invention. According to Sharrit or Kazmierski, the method includes steps

Performing a standard transient analysis algorithm including Newton-Raphson iteration (col. 6, lines 22-43, for example), (Kazmierski, cols. 6-7),

Performing a regular iterative equation solution process (col. 3, lines 7-42, col. 5, lines 31-43, for example), see Kazmierski also, cols. 6-10,

Performing process iteration at an accepted timepoint (col. 6, lines 21-43, col. 8, lines 43-59, for example), and user interacting with the process simulation during the iteration taking place (col. 5, line 30 to col. 6, line 44, col. 7, lines 3-55, col. 10, lines 33-50). Sharrit and Kazmierski do not expressly disclose the claimed limitation of a replay of the last iteration. Such claimed replay of the iteration is well-known in the art. In

fact, On teaches means and step to perform a replay of iteration for independent process debugging and dynamically view or examine the debugging process (col. 4, lines 21-61, col. 5, lines 1-40).

This would motivate practitioner in the art at the time of the invention was made to combined the teaching of iteration process replay in On into Sharrit or Kazmierski simulation above in order to independently debug process error and dynamically examine process debugging by taking an effective way of replay of the simulation iteration at the selected timepoint to improve simulation resolution as taught in On.

As per claim 3, Sharrit/Kazmierski disclose step: single stepping through the simulation for interactively debugging a behavioral model (cols. 6 and 10).

As per claim 4, the prior art of record discloses process debugging in timepoints as claimed.

As per claims 5-6, On teaches debug trigger for debugging event as claimed.

As per claim 14, Sharrit and Kazmierski disclose computer readable media for simulating a circuit with feature limitations very similar to the claimed invention. According to Sharrit/Kazmierski, the simulation readable medium includes means and functional steps

Performing a standard transient analysis algorithm including Newton-Raphson iteration (col. 6, lines 22-43, for example), also see Kazmierski, cols. 6-7,

Performing a regular iterative equation solution process (col. 3, lines 7-42, col. 5, lines 31-43, for example), (Kazmierski, cols. 6-10),

Performing process iteration at an accepted timepoint (col. 6, lines 21-43, col. 8, lines 43-59, for example), and user interacting with the process simulation during the iteration taking place (col. 5, line 30 to col. 6, line 44, col. 7, lines 3-55, col. 10, lines 33-50) and Kazmierski, cols. 6-10 above. Sharrit and Kazmierski do not expressly disclose the claimed limitation of a replay of the last iteration. Such claimed replay of the iteration is well-known in the art. In fact, On teaches means and step to perform a replay of iteration for independent process debugging and dynamically view or examine the debugging process (col. 4, lines 21-61, col. 5, lines 1-40).

This would motivate practitioner in the art at the time of the invention was made to combined the teaching of iteration process replay in On into Sharrit/Kazmierski simulation medium in order to independently debug process error and dynamically examine process debugging by interactively replaying debug process for a specific timepoint as taught in On.

As per claim 15, Sharrit/Kazmierski discloses step of by single stepping through the simulation for interactively debugging a behavioral model (cols. 6 and 10).

As per claim 16, the prior art of record discloses process debugging in timepoints as claimed.

As per claims 17-18, On teaches debug trigger for debugging event as claimed.

As per claim 19, On teaches downloading software program over an internet from a website as claimed.

Allowable Subject Matter

1. Claims 7-12 and 20-26 are allowable. The following is an examiner's statement of reasons for allowance:

2. The claimed invention is directed to a method and system for debugging signal behavior models of circuit designs and simulation using Newton-Raphson iteration replay. The claimed simulator includes means and step for interactive replay model behavior verification, verifying model behaviors convergence using Newton-Raphson iteration to derive an acceptable timepoint for single stepping statement or sequential statement breakpoints as claimed.

Response to Arguments

Applicant's arguments filed 02/18/2005 have been fully considered but they are not persuasive.

In response to applicant's argument Sharrit, Vlach, or Kazmierski does not disclose the claimed step "performing a replay of the last Newton-Raphson iteration of an accepted timepoint" in claim 1, the examiner reminds such feature is not present in the claim for consideration.

In response to applicant's argument the combined prior art Sharrit, Vlach, or Kazmierski in view of On does not disclose the claimed step "performing a replay of the last Newton-Raphson iteration of an accepted timepoint" in independent claim 2, the examiner responds Sharrit, Vlach, and Kazmierski disclose the well-known Newton-Raphson iteration in circuit simulation. For replay of the iteration at an accepted

timepoint, the examiner shown On disclosed such feature for replaying captured events, iteration events, etc as in col. 4, lines 21-61, cols. 5-6.

In response to applicant's argument On is not a related art to design and verification technology, the examiner disagrees with. On disclosure is a method and apparatus for debugging programs such as simulation program. On discloses the program debugger utilizes a replay process for dynamic visual parallel debugging a program event, showing the execution of the program under simulation, etc. This technique provides advantages to the related arts and technology such as system simulation and program development.

This would motivate practitioner in the art at the time of the invention was made to combined the teaching of iteration process replay in On into Sharrit or Kazmierski simulation above in order to independently debug process error and dynamically examine process debugging by taking an effective way of replay of the simulation iteration at the selected timepoint to improve simulation resolution as taught in On.

Conclusion

1. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

1. US patent no. 5,995,733, issued to Roychowdhury, Jaijeetl, on July 2001

2. US patent no. 6,530,065 B1, issued to McDonald et al, on Mar. 2003

THIS ACTION IS MADE FINAL. Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

2. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Thai Q. Phan whose telephone number is 571-272-3783. The examiner can normally be reached on Monday-Friday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Jean Homere can be reached on 571-272-3780. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

3. Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

June 07, 2005

Thai Phan

Patent Examiner